WHAT IS CLAIMED IS:

1. A nonvolatile memory system comprising:

one or more semiconductor memories; and

an information processor for reading data stored in said one or more semiconductor memories, giving a data writing operation instruction or performing a predetermined process on the basis of an operation program,

wherein when an emergency stop signal is received from the outside, said information processor stops an operation being performed and enters a no-response state in which no response is given to a process request from the outside.

2. The nonvolatile memory system according to claim 1, wherein the no-response state of said information processor is canceled by re-start of said nonvolatile memory system.

3. A nonvolatile memory system comprising:

one or more semiconductor memories; and

an information processor for reading data stored in said one or more semiconductor memories, giving a data writing operation instruction or performing a predetermined process on the basis of an operation program,

wherein said information processor includes:

a power supply voltage unit for generating an internal power supply voltage from an external power supply voltage and supplying the internal power supply voltage to said semiconductor memory and said information processor;

a first voltage monitoring unit for outputting a power-on-reset signal when the internal power supply voltage generated by said power supply voltage unit becomes at a first voltage level; and

a second voltage monitoring unit for outputting an emergency stop signal when the external power supply voltage becomes at a second voltage level, and

wherein when the emergency stop signal output from said second voltage monitoring unit is received, said information processor stops an operation being performed and enters a no-response state in which no response is given to a process request from the outside, and when the power-on-reset signal output from said first voltage monitoring unit is received, said information processor performs a resetting process.

4. A nonvolatile memory system comprising:

one or more semiconductor memories; and

an information processor for reading data stored in said one or more semiconductor memories, giving a data writing operation instruction or performing a predetermined process on the basis of an operation

program,

wherein said information processor includes:

a power supplying unit for supplying an auxiliary power supply voltage;

a power supply switching unit for outputting an emergency stop signal when an external power supply voltage becomes at a first voltage level, switching said external power supply voltage to the power supply voltage of said power supplying unit and supplying the power supply voltage to said semiconductor memory and said information processor; and

a first voltage monitoring unit for outputting a power-on-reset signal when said external power supply voltage becomes at a second voltage level,

wherein when the emergency stop signal output from said power supply switching unit is received, said information processor stops an operation being performed and enters a no-response state in which no response is given to a process request from the outside, and when the power-on-reset signal which is output from said first voltage monitoring unit is received, said information processor performs a resetting process.

5. The nonvolatile memory system according to claim 4, wherein when said emergency stop signal is received during a data transfer process in a reading or writing operation, said information processor finishes the data

transfer process safely and, after that, enters said no-response state.

6. The nonvolatile memory system according to claim 5, wherein in said no-response state, said information processor notifies a host which is externally connected of either an end, an error, or a busy state.

7. A nonvolatile memory system comprising:

one or more semiconductor memories; and

an information processor for reading data stored in said one or more semiconductor memories, giving a data writing operation instruction or performing a predetermined process on the basis of an operation program,

wherein said information processor has a transfer mode storing unit for storing transfer function setting data for setting a transfer mode of error data, refers to the transfer function setting data in said transfer mode storing unit in a data transfer process at the time of a read operation or a write operation and, when an error data transfer function of said transfer function setting data is set to be valid, executes a transfer process even if transfer data includes error data.

8. The nonvolatile memory system according to claim 7, wherein said transfer mode storing unit takes the form

of a register, and said transfer function setting data is set by a command which is received from the outside.

9. The nonvolatile memory system according to claim 7,

wherein said transfer mode storing unit is a memory area as a part of said semiconductor memory, and

wherein said information processor refers to the transfer function setting data stored in the memory area in said semiconductor memory at the time of data transfer and, in the case where an error data transfer function is set to be valid, executes a transfer process even if transfer data includes error data.

10. The nonvolatile memory system according to claim 8,

wherein said information processor has an error data detecting and correcting unit for correcting error data, and

wherein said error data detecting and correcting unit detects whether error data is included in said transfer data or not, if error data is included in said transfer data and said error data is correctable, corrects said error data and transfers the corrected data and, if said error data is uncorrectable, said error detecting and correcting unit transfers said error data without correcting it.

11. A nonvolatile memory system comprising:

one or more semiconductor memories; and

an information processor for reading data stored in said one or more semiconductor memories, giving a data writing operation instruction or performing a predetermined process on the basis of an operation program,

wherein an error determining unit is provided for determining whether an error is included in data read from said semiconductor memory or not at the time of reading from said semiconductor memory, and

wherein the system has a first reading operation for determining whether an error is included in data read from said semiconductor memory or not by said error determining unit and outputting the data, and a second reading operation for outputting the read data without determining whether an error is included or not.

12. The nonvolatile memory system according to claim 11,

wherein said error determining unit has an error correcting function, and

wherein, in the case where it is determined that an error is included in data read from said semiconductor memory in said first reading operation, the error is corrected by said error correcting function.

13. The nonvolatile memory system according to claim 12, wherein in said first reading operation, when an error detected in data read from said semiconductor memory can be corrected by said error correcting function, said error determining unit corrects the error and, when an error is uncorrectable within predetermined time, said error determining unit does not correct the error.

14. The nonvolatile memory system according to claim 13, wherein in said first reading operation, when an error which cannot be corrected within predetermined time is detected in data read from said semiconductor memory, said error determining unit outputs the data read from said semiconductor memory without correcting the error.